Form PTO-1449 (Modified)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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Atty. Docket No.	Serial No.
1662-37200 (P00-3159)	09/838,078
Applicants: Shubhendu S. MUKHERJEE et al.	
Filing Date: April 19, 2001	Group: 2182

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
BJO	AA	5,758,142	05/26/98	McFarling et al.	395	586	05/31/94
BJO	AB	5,933,860	08/03/99	Emer et al.	711	213	07/29/97

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	Translation NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

BJO	AC	M. Franklin, "Incorporating Fault Tolerance in Superscalar Processors," Proceedings of High Performance Computing, December, 1996.
BJO	AD	A. Mahmood et al., "Concurrent Error Detection Using Watchdog Processors - A Survey," IEEE Trans. on Computers, 37(2):160-174, February 1988.
BJO	AE	J. H. Patel et al., "Concurrent Error Detection In ALU's by Recomputing With Shifted Operands," IEEE Trans. on Computers, 31(7):589-595, July 1982.
BJO	AF	D. A. Reynolds et al., "Fault Detection Capabilities Of Alternating Logic," IEEE Trans. on Computers, 27(12):1093-1098, December 1978.
BJO	AG	E. Rotenberg et al., "Trace Cache: A Low Latency Approach To High Bandwidth Instruction Fetching," Proceedings of the 29th Annual International Symposium on Microarchitecture, pp. 24-34, December 1996.
BJO	AH	E. Rotenberg et al., "Trace Processors," 30th Annual International Symposium on Microarchitecture (MICRO-30), Dec. 1997.
BJO	AI	T. J. Slegel et al., "IBM's S/390 G5 Microprocessor Design," IEEE Micro, pp. 12-23, March/April 1999.
BJO	AJ	J. E. Smith et al., "Implementing Precise Interrupts In Pipelined Processors," IEEE Trans. on Computers, 37(5):562-573, May 1988.
BJO	AK	G. S. Sohi et al., "A Study Of Time-Redundant Fault Tolerance Techniques For High-Performance Pipelined Computers," Digest of Papers, 19th International Symposium on Fault-Tolerant Computing, pp. 436-443, 1989.
BJO	AL	G. S. Sohi et al., "Instruction Issue Logic For High-Performance, Interruptible, Multiple Functional Unit, Pipelined Computers," IEEE Transactions on Computers, 39(3):349-359, March 1990.
BJO	AM	D. M. Tullsen, et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture, Italy, June 1995.
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BJO	AO	S. K. Reinhardt et al., "Transient Fault Detection Via Simultaneous Multithreading" (12 p.).
BJO	AP	L. Spainhower et al., "IBM S/390 Parallel Enterprise Server G5 Fault Tolerance: A Historical Perspective," IBM J. Res. Develop. Vol. 43, No. 5/6, September/November 1999, pp. 863-873.
BJO	AQ	M. Franklin, "A Study Of Time Redundant Fault Tolerance Techniques For Superscalar Processors" (5 p.).
BJO	AR	K. Sundaramoorthy et al., "Slipstream Processors: Improving Both Performance And Fault Tolerance" (6 p.).

EXAMINER _____ **DATE CONSIDERED** 4/9/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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1662-37200 (P00-3159)	Not Yet Assigned
Applicants	
Shubhendu S. MUKHERJEE et al.	
Filing Date	**Group**
Concurrently Herewith	Unknown

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	Translation YES	Translation NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

BSO	AA	*AR-SMT: Microarchitectural Approach To Fault Tolerance In Microprocessors*, Eric Rotenberg, (8 p.).
BSO	AB	*DIVA: A Dynamic Approach To Microprocessor Verification*, Todd M. Austin, Journal of Instruction-Level Parallelism 2 (2000) 1-6, Submitted 2/2000; published 5/2000 (26 p.).
BSO	AC	*DIVA: A Reliable Substrate For Deep Submicron Microarchitecture Design*, Todd M. Austin, May/June 1999 (12 p.).

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